Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the applications:

Listing of Claims:

1-11. (Canceled)

12. (Currently Amended) A program of instructions stored ~~storable~~ on a medium, executable[[ed]] by a computer, the program of instructions comprising:

creating a first state;

creating a second state;

~~applying a layer of abstraction to multiple parameters;~~

building a state machine from the first and second states, the state machine being capable of executing ~~at least one~~ a plurality of functions, each of the ~~at least one~~ plurality of functions being implemented in code common to ~~the~~ multiple parameters and specific to each of the ~~at least one~~ plurality of functions, wherein the ~~at least one~~ plurality of functions includes at least one selected from the group consisting of editing, storing, loading, and displaying; ~~and~~

~~performing one selected from the group comprising testing, validating, and simulating a device under test~~

loading test parameters of the multiple parameters for a test through utilization of one of the plurality of functions of the state machine;

performing the test with current values of the test parameters through utilization of the state machine;

determining whether the test is complete;

varying a value of one of the test parameters within a boundary of the one of the test parameters through utilization of one of the plurality of functions of the state machine and testing with the current values of the test parameters through

utilization of the state machine until the test is complete; and

logging at least one state change of the state machine that occurs during the test.

13. (Canceled)

14. (Previously Presented) The program of instructions of Claim 12, wherein the multiple parameters include a Peripheral Component Interconnect (PCI) cache line size.

15. (Previously Presented) The program of instructions of Claim 12, wherein the multiple parameters include a Small Computer System Interface (SCSI) synchronous rate.

16. (Previously Presented) The program of instructions of Claim 12, wherein the multiple parameters include a block size.

17. (Previously Presented) The program of instructions of Claim 12, further comprising a look up table for storing default values of the multiple parameters.

18. (Previously Presented) The program of instructions of Claim 12, further comprising a look up table for providing type and value information for each of the multiple parameters.

19. (Previously Presented) The program of instructions of Claim 18, wherein the type and value information includes a range of values that are permitted for each of the multiple parameters.

20. (Previously Presented) The program of instructions of Claim 19, wherein the type and value information includes an incremental step size for each of the multiple parameters.

21. (Previously Presented) The program of instructions of Claim 12, wherein at least one of the multiple parameters is independent of type.

22-43. (Canceled)

44. (Currently Amended) The program of instructions of Claim 12, further comprising:

adding at least one new parameter to the multiple parameters~~; and applying the same layer of abstraction to the at least one new parameter that was applied to the multiple parameters~~.

45. (Previously Presented) The program of instructions of Claim 12, further comprising:

performing one selected from adding, changing, and deleting at least one state from the state machine.

46. (Previously Presented) The program of instructions of Claim 12, further comprising:

utilizing the state machine to perform system level validation of new silicon.

47. (Currently Amended) The program of instructions of Claim 12, wherein building the state machine further comprises importing parameter information into the code common to the multiple parameters and specific to each of the ~~at least one~~ plurality of functions.

48. (Previously Presented) The program of instructions of Claim 12, wherein the state machine is independent of bus type.

49. (Previously Presented) The program of instructions of Claim 12, further

comprising a second state machine interrelated with the state machine.

50. (Currently Amended) The program of instructions of Claim 12, wherein pointers and status functions are utilized to build and maintain the state ~~status~~ machine.